WEST Search History

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Primary Examiner

DATE: Monday, December 01, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=JPAB; PLUR=YES; OP=ADJ			
L13	boundary addess decoder	0	L13
L12	L11 and decoder	1	L12
L11	memory and boundary adj2 address$1	90	L11
L10	memory and boundary adj2 (offset or address$1)	91	L10
DB=USPT,PGPB; PLUR=YES; OP=ADJ			
L9	6446195	11	L9
L8	09/494608	9	L8
L7	L4 and boundary adj2 address$1	2	L7
L6	L5 and offset address$1	0	L6
L5	L4 and boundary	15	L5
L4	L3 and left adj3 (row$1 or array$1 or block$1)	75	L4
L3	L2 and right adj3 (row$1 or array$1 or block$1)	100	L3
L2	row address decoder	1769	L2
L1	memory adj1 (block$1 or array$1)	36204	L1

END OF SEARCH HISTORY

WEST

Generate Collection

L12: Entry 1 of 1 File: JPAB Nov 11, 1997

PUB-NO: JP409293020A
DOCUMENT-IDENTIFIER: JP 09293020 A
TITLE: INTERFACE CIRCUIT

PUBN-DATE: November 11, 1997

INVENTOR-INFORMATION:
NAME COUNTRY
KOBAYASHI, HIROYUKI
SHIMIZU, YASUSHI
SAWADA, MICHIYA

ASSIGNEE-INFORMATION:
NAME COUNTRY
OKI ELECTRIC IND CO LTD

APPL-NO: JP08105943
APPL-DATE: April 26, 1996

INT-CL (IPC): G06 F 12/14; G06 F 12/00

ABSTRACT:

PROBLEM TO BE SOLVED: To provide an interface circuit whereby the overflow of a stack area is quickly detected and the influence of a fault on the whole system is made to be min.

SOLUTION: An I/F circuit 50 is provided with a decoder 51 which decodes address data, transmits it to a memory device 3 as a memory access signal 61 and also stops the transmission of the memory access signal 61 when a memory access restricting signal 64 is received from a comparing circuit 53, an address register 52 which stores an address value indicating the boundary of the stack area as a stack area boundary address value 63 and the comparing circuit 53 which normally compares the address to be transmitted to an address bus 11 by a microprocessor 1 with the stack area boundary address value 63. Then, the microprocessor 1 sets the boundary address of the stack area, recognizes the overflow of a stack when the access address of the microprocessor 1 exceeds the set boundary address and executes the bus-error completion of the access.